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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/067,599 04/28/98 ALLISON

S RA998-007

LM12/0502
JOSCELYN G COCKBURN
IBM CORPORATION 972/B656
P O BOX 12195
RESEARCH TRIANGLE PARK NC 27709

EXAMINER

CHANNAVAT TALA, S

ART UNIT	PAPER NUMBER
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2777

DATE MAILED:

05/02/00

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/067,599	Applicant(s) Allison et al.,
	Examiner Srirama Channavajjala	Group Art Unit 2777

Responsive to communication(s) filed on 4/28/1998

This action is FINAL.

Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

Claim(s) 1-14 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

Claim(s) _____ is/are allowed.

Claim(s) 1-14 is/are rejected.

Claim(s) _____ is/are objected to.

Claims _____ are subject to restriction or election requirement.

Application Papers

See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

The drawing(s) filed on _____ is/are objected to by the Examiner.

The proposed drawing correction, filed on Apr 28, 1998 is approved disapproved.

The specification is objected to by the Examiner.

The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

All Some* None of the CERTIFIED copies of the priority documents have been

received.

received in Application No. (Series Code/Serial Number) _____.

received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

Notice of References Cited, PTO-892

Information Disclosure Statement(s), PTO-1449, Paper No(s). 2

Interview Summary, PTO-413

Notice of Draftsperson's Patent Drawing Review, PTO-948

Notice of Informal Patent Application, PTO-152

-- SEE OFFICE ACTION ON THE FOLLOWING PAGES --

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DETAILED ACTION

1. Claims 1-14 are presented for examination.

Drawings

2. The Drawing filed on 4/28/98 are not objected to by the Draftsperson under 37CFR 1.84 or 1.152, [see PTO-948, paper no.# 3].

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Information Disclosure Statement

4. The information disclosure statement filed on 4/28/1998, paper no. # 2 has been considered and a copy is hereby enclosed.

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Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371[®] of this title before the invention thereof by the applicant for patent.

6. Claims 1-8, 12-14 rejected under 35 U.S.C. 102(e) as being anticipated by .

Dea et al., [hereafter Dea], US Patent No. 5742833.

7. As to Claim 1, Dea details a system in which 'a network interface card' [col 6, line 3-7, line 51-55], examiner interpreting network interface card to be equivalent to Dea's Ethernet network card, 'system interface circuit arrangement' [fig 1-3, col 5, line 30-52], 'network interface circuit arrangement' [fig 3, col 6, line 39-57, col 6, line 51-57], 'a storage for storing a set of patterns' [fig 1, element 14, col 5, line 18-24, col 10, line 65-67, col 11, line 1-4, col 11, line 1-4], 'a pattern match logic circuit arrangement correlating marked patterns with other data and generating at least one first control signal if a match occurs between one of the marked patterns' [col 11, line 7-42, line 62-67].

8. As to Claim 2, Dea details a system which including 'a host computer coupled to the system interface' [fig 1, col 4, line 61-67, col 5, line 1-6], 'host computer including software for downloading' [col 6, line 12-21], 'network interface card the set of patterns and the mask data' [col 3, line 64-67].

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9. As to Claim 3, Dea details a system which including ‘address matching function logic circuit for correlating an address for the network interface card and a received address and generating a second control signal on the occurrence of a match’ [col 3, line 44-51].

10. As to Claim 5, Dea details a system which including ‘patterns are arranged contiguously in the mask storage’ [fig 6, col 9, line 6-10, line 64-67, col 10, line 1-4].

11. As to Claims 6-7, Dea details a system which including ‘mask data is arranged so that each m-bits word of mask contains mask bits for words in N patterns’ [figs 5-6, col 9, line 64-67, col 10, line 1-11].

12. As to Claim 8, Dea details a system which including ‘pattern match logic circuit arrangement includes a first state machine for assembling data received from the network interface circuit arrangement’ [col 10, line 12-41, col 11, line 45-63], ‘a second state machine coupled to the first state machine, said second state including means for receiving the predetermined sizes from the first state machine and generating addresses for accessing the pattern storage’ [col 10, line 12-41, col 11, line 62-67, col 12, line 1-17].

13. As to Claim 12, Dea details a system which including ‘pattern matching’ [col 4, line 44-47], ‘providing a set of patterns’ [col 8, line 55-67], ‘providing a set of data’ [col 8, line 55-67], ‘providing mask for identifying portions of the patterns’ [col 8, line 55-67, col 9, line 6-17], ‘correlating data from the set of data with identified portions’ [col 9, line 33-39], ‘generating a match signal, identified portion of the pattern match’ [col 9, line 55-67, col 10, line 1-4].

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14. As to Claim 13, Dea details a system which including ‘communications network to wake station connected to the communications network’ [fig 1, see Abstract], ‘network interface card’ [col 6, line 3-7, line 51-55, see fig.2-3], examiner interpreting network interface card to be equivalent to Dea’s Ethernet network card, ‘set of patterns against which data from the communications network is to be matched’ [col 3, line 52-67], ‘mask data indicating portions of a pattern to be used’ [col 8, line 55-67, col 9, line 6-17, col 10, line 12-14], ‘correlating each identified portion with data received from the communications network’ [col 9, line 33-39], examiner interpreting communication network to be equivalent to Dea’s fig 1., ‘generating a wake-up signal if a match occurs’ [col 9, line 43-49].

15. As to Claim 14, Dea details a system which including ‘station address with an address received with the data from the communications network’ [fig 5, col 7, line 66-67, col 8, line 1-16].

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Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103[®] and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

17. Claims 4, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dea et al., [hereafter Dea], US Patent No. 5742833.

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18. As to Claim 4, Dea specifically not detailed 'each pattern in the set of patterns are arranged in 4 byte wide words and 128 byte sectors', however, Dea suggested frame data fields of network packets having different sizes can be implemented for example as shown in fig 5-6.

It would have been obvious of the ordinary skill in the art at the time of applicant invention to arranging various different byte size words and byte sectors because it not only provides flexibility, but also, saves memory space, thus improving the responsiveness of the system.

19. As to Claim 9, Dea does not detail 'address generation means uses the expression YYYxxxxx to determine the addresses for the pattern RAM, wherein xxxx represents an index count and YYY represents states for a state machine.', although Dea suggested for example using specific network protocol network IEEE Ethernet 48 bit address [see col 2, line 1-13].

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to assign one bit or multiple bits 'Y' for state machine, multiple bits 'x' for index count because predetermined address of one bit or multiple bits saves memory space, improving the pattern matching and responsiveness of the system.

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20. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dea et al [hereafter Dea], US Patent No. 5742833 as applied to claim 1 above, and further in view of Jeng, US Patent No. 5892768.

21. As to Claims 10-11, Dea does not specifically detail ‘PCI interface’ and ‘Ethernet MII interface’, although Dea suggested using IEEE Ethernet and/or Ethernet protocol, also related Ethernet controller mechanisms having network interface controller for example shown in fig 2. see col 6, line 3-12. Jeng details a system in which ‘PCI interface’ and ‘Ethernet MII interface’ [fig 2-3, fig 7, col 6, line 13-27].

It would have been obvious one of the ordinary skill in the art at the time of the applicant invention to combine the concepts taught by Jeng with the system of Dea because, PCI interface provides high bandwidth, and connecting through PCI buses bringing the advantages of fast exchange of data because PCI is typically 32-bit or 64-bit at 33 MHZ speed, thus improving the response time and efficiency of the system.

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Conclusion

The prior art made of record

- a. US Patent No. 5742833
- b. US Patent No. 5892768

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- c. US Patent No. 6016401
- d. US Patent No. 6012100
- e. US Patent No. 5802287
- f. US Patent No. 5835719
- g. US Patent No. 5802305

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srirama Channavajjala whose telephone number is (703)308-8538. The examiner can normally be reached on Monday-Friday from 7:00 AM to 3:30 PM Eastern time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Breene, can be reached on (703)305-9790. The fax phone number for this Art Unit is (703)308-5403

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703)305-9600.

cs

April 28, 2000


JOHN E. BREENE
PRIMARY EXAMINER